Machine Learning Models for Improving Productivity in ASIC Design Flow

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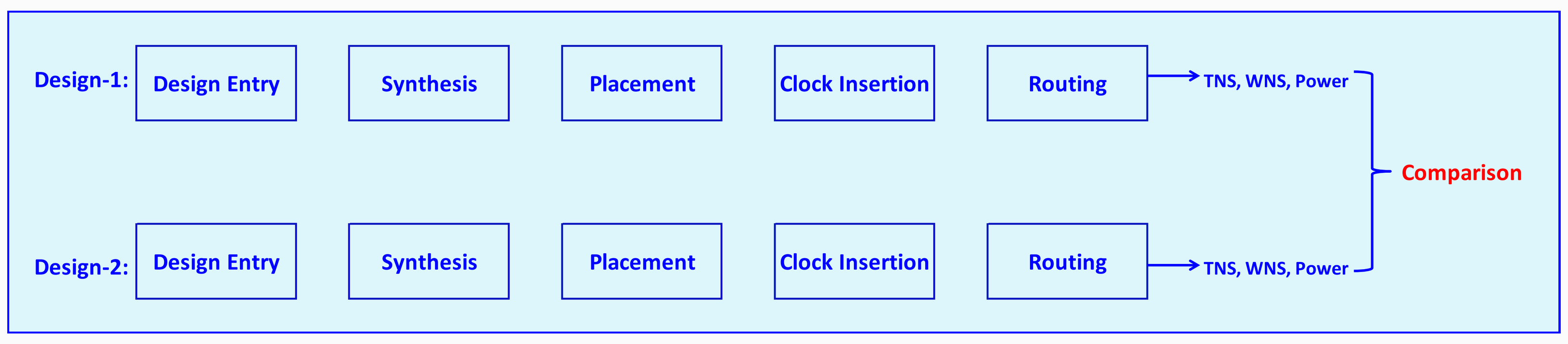
Motivation

- To achieve target Power-Performance-Area (PPA) within the goal-to-market constraint, ASIC Physical Implementation (PI) engineers run parallel experiments that target different aspects of design and/or tool settings.
- Experiments go through time-consuming and computationally expensive steps: synthesis, place, clock-insertion, route. Typical large designs may take 4-5 days to go from place to route.



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Motivation (Contd.)

- Rather than waiting on the final routed designs, PI engineers spend significant time to identify which of the parallel experiments will be the best one. They then pursue further improvement on those experiments. Furthermore, once the route step is finished, designers' assumptions may be proven to be incorrect.
- We propose a Machine Learning (ML) based model "**CompareApp**" to facilitate early and more correct comparison of the experiments that the designers run. Our model essentially targets a classification problem.

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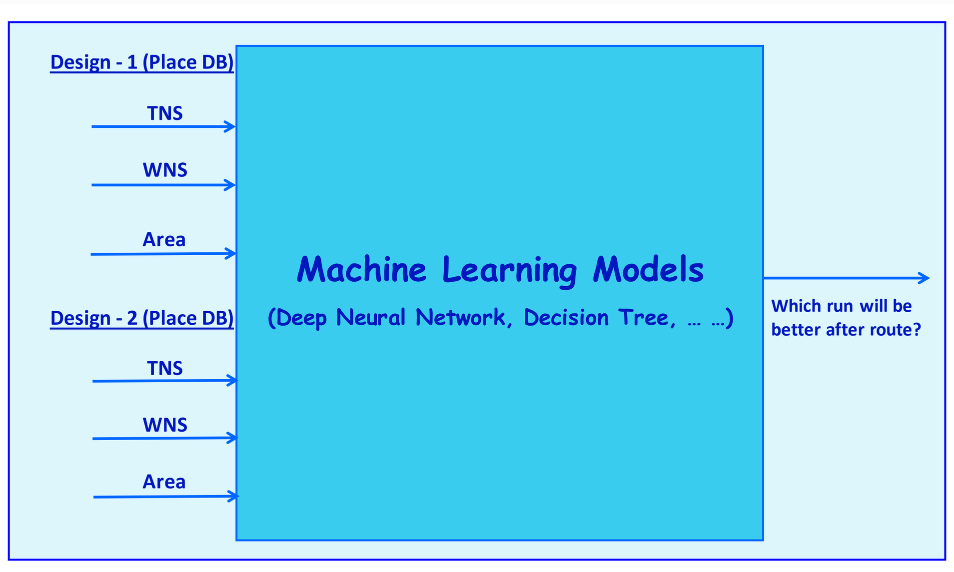
Proposed Model

- CompareApp compares two runs after place and predicts which run will be the best after final step (route)
- ML models investigated:
  - Support Vector Machine
  - Decision Tree
  - Multilayer Perceptron
  - Deep Neural Network



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Methodology / Experimental Setup

- **Inputs:** Quality metrics for two placed databases as inputs: worst negative slack (WNS), total negative slack (TNS), area etc. We use a total of 84 features for two runs combined.
- **Training & Testing data:** We *randomly* choose 90% of data for training and the remaining 10% of data for testing.
- **Output:** Prediction of which run is better after the route step. We currently use only TNS for comparison.
- **Tools used:**
  - Commercially available place-and-route tool for actual data.
  - We implement our model using an ML platform, which we are developing in collaboration with Inzone.ai.

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Experimental Results

Design	Cell count	Area	Commercial tool Flow-Time: place to route with clock	Accuracy (DNN)	Accuracy (Decision Tree)
Design-1	780,000	205,000	110 Hours	94.20%	89.01%
Design-2	675,000	115,000	80 Hours	91.72%	89.22%
Design-3	310,000	64,000	40 Hours	92.96%	90.94%
Design-4	343,000	75,000	50 Hours	92.86%	88.84%
Design-5	454,000	108,000	100 Hours	93.49%	90.42%
Design-6	197,000	30,000	30 Hours	93.68%	90.50%
Design-7	255,000	77,000	35 Hours	94.57%	86.98%
Design-8	380,000	78,000	50 Hours	92.33%	90.05%
Design-9	690,000	362,000	65 Hours	92.03%	87.37%
Average				**93.09%**	**89.26%**

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Conclusion / Future Work

- We propose an ML-based technique, CompareApp that can use placed information to predict the best run out of a set of parallel runs
- We got 92%-95% accuracy across the nine designs that we investigated. Deep Neural Network (DNN) based technique gave the best accuracy. Our model worked fine on the corner cases.
- **Future Work:**
  - Extension of the model to compare more than two runs
  - Extension of the model to make comparisons in regards to other metrics, such as power, area, WNS
  - Extension of the model to predict better routed design immediately after the synthesis step

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